CLAIMS

What is claimed is:

1. A method of concurrently forming two doped regions in a semiconductor substrate, comprising:

forming a mask layer over a semiconductor substrate having a first conductivity type;

patterning the mask layer to form two openings therein, wherein a first opening is larger than a second opening, and wherein the first opening is larger than a second opening, and wherein the first opening is larger than an implantation design rule, and the second opening is less than the implantation design rule; and

selectively implanting the semiconductor substrate with ions of a second conductivity type through the openings in the patterned mask layer, thereby defining a first implanted region associated with the first opening and having a first depth associated therewith and a second implanted region associated with the second opening and having a second depth associated therewith, and wherein the first depth is greater than the second depth.

2. The method of claim 1, wherein the mask layer comprises a photoresist.

3. The method of claim 1, wherein the first conductivity type comprises p-type and the second conductivity type comprises n-type.

4. The method of claim 1, wherein the total dopant in the first region is higher than the total dopant in the second region due to the first opening being larger than the design rule and the second opening being smaller than the design rule, and further comprising annealing the substrate, wherein the first region diffuses a distance which is greater than a diffusion distance of the second region, resulting in the first depth being greater than the second depth.

5. A method of forming a bipolar transistor in a BiCMOS process, comprising:

forming a patterned buried layer mask over a semiconductor substrate, the substrate having a first conductivity type, wherein the patterned buried layer mask comprises a plurality of openings therein, and wherein each of the plurality of openings are smaller than a distance required by an implantation design rule;

performing a buried layer implant into the substrate with ions of a second conductivity type through the openings in the patterned buried layer mask, resulting in a plurality of distinct implanted regions in the substrate corresponding to the openings;

thermally processing the substrate after the buried layer implant, wherein the implanted regions laterally diffuse together to form a buried layer of the second conductivity type in the substrate;

forming a semiconductor layer of the first conductivity type over the buried layer and the substrate, the semiconductor layer forming a base region;

selectively implanting a deep collector region of the second conductivity type into the semiconductor layer, the deep collector region extending down and coupling to a portion of the buried layer, wherein the deep collector region and the buried layer together form a collector of the bipolar transistor;

selectively performing a source/drain implant of the second conductivity type into the semiconductor layer, the source/drain implant forming an emitter region within the base region, and wherein a distance between a bottom portion of the emitter and a top portion of the buried layer influences a collector-to-emitter breakdown voltage of the bipolar transistor.

6. The method of claim 5, wherein the first conductivity type is p-type and the second conductivity type is n-type, thereby defining an NPN type bipolar transistor.

7. The method of claim 5, wherein the patterned buried layer mask comprises a photoresist.

8. The method of claim 5, wherein selectively implanting the deep collector region further comprises implanting a ring of the deep collector into the semiconductor layer and down to the buried layer, the p-type region surrounded by the deep collector ring defining an area of the base region.

9. The method of claim 5, wherein forming the patterned buried layer mask further comprises forming another opening therein, wherein the another opening is larger than the distance required by the implantation design rule.

10. The method of claim 9, wherein the buried layer implant implants ions of the second conductivity type into the semiconductor layer through the another opening, and the annealing of the substrate causes the ions to diffuse a distance into the substrate that is greater than a diffusion distance associated with the buried layer.

11. The method of claim 10, wherein processing performed subsequent to the buried layer implant causes the ions in the semiconductor layer associated with the buried layer and the another opening to diffuse up into the semiconductor layer, and wherein a diffusion distance associated with the ions of the another openings is greater than a diffusion distance of the buried layer.

12. The method of claim 5, wherein forming the semiconductor layer comprises depositing the semiconductor layer over the semiconductor substrate and the buried layer via an epitaxial growth process, wherein the semiconductor layer is an epi layer of the first conductivity type.

13. A method of forming a bipolar transistor in a BiCMOS process, comprising:

forming a buried layer of a second conductivity type in a semiconductor substrate of a first conductivity type;

forming an epi layer of the first conductivity type over the buried layer and the semiconductor substrate with epitaxial growth process;

forming a deep collector region of the second conductivity type in the epi layer, the deep collector region extending down and coupling to a portion of the buried layer;

forming a deep well region of the second conductivity type in the epi layer, the deep well region extending down to the buried layer and extending laterally to the deep collector region ,wherein the deep well region, the deep collector region and the buried layer together form a collector of the bipolar transistor;

forming a shallow well mask on the epi layer, the shallow well mask having a plurality of openings overlying the deep well region in the epi layer, wherein at least one of the openings is smaller than distance required by an implantation design rule;

selectively implanting ions of a first conductivity type into the deep well region through the plurality of openings in the shallow well mask, resulting in a plurality of distinct implanted regions in the deep well region corresponding to the openings;

thermally processing the substrate, wherein the implanted regions laterally diffuse together to form a shallow well region of the first conductivity type within the deep well region of the second conductivity type, the shallow well region forming a base region within the collector region; and

selectively performing a source/drain implant of the second conductivity type into the shallow well region, the source/drain implant forming an emitter region within the base region of the bipolar transistor.

14. The method of claim 13, wherein forming the buried layer comprises selectively implanting ions of the second conductivity type into the substrate through a patterned mask.

15. The method of claim 13, wherein the shallow well mask has at least two openings associated therewith, wherein a first opening is associated with an extrinsic portion of the base region and has a size which is greater than the distance required by the implantation design rule, and wherein a second opening is associated with an intrinsic portion of the base region and has a size which is less than the distance required by the implantation design rule.

16. The method of claim 15, wherein selectively implanting ions into the deep well region through the shallow well mask comprises concurrently exposing both the first and second openings to an implantation dose, wherein a resultant concentration of ions in a first region of the deep well region corresponding to the first opening is greater than a concentration of ions in a second region of the deep well region corresponding to the second opening.

17. The method of claim 16, wherein thermally processing the substrate causes ions in the first region and the second region to laterally diffuse together resulting in the shallow well region, and wherein the ions in the first region diffuse vertically a greater distance than a vertical diffusion of ions in the second region, resulting in the shallow well region having a depth in the extrinsic region of the base which is greater than a depth in the intrinsic region of the base.

18. The method of claim 17, wherein the source/drain implant forming the emitter is performed in the intrinsic region of the base, and wherein a distance between a bottom portion of the emitter and a bottom portion of the intrinsic region of the base influence a gain of the bipolar transistor.

19. The method of claim 13, wherein the first conductivity type is p-type and the second conductivity type is n-type, resulting in an NPN bipolar transistor.

20. A method of forming a bipolar transistor in a BiCMOS process, comprising:

forming a buried layer of a second conductivity type in a semiconductor substrate of a first conductivity type;

forming an epi layer of the first conductivity type over the buried layer and the semiconductor substrate with an epitaxial growth process;

forming a deep collector region of the second conductivity type in the epi layer, the deep collector region extending down and coupling to a portion of the buried layer;

forming a deep well region of the second conductivity type in the epi layer, the deep well region extending down to the buried layer and extending laterally to the deep collector region, wherein the deep well region, the deep collector region and the buried layer together form a collector of the bipolar transistor;

forming a shallow well region of the first conductivity type within the deep well region, the shallow well region forming a base region of the bipolar transistor;

forming an emitter mask over the substrate, the emitter mask having a first opening located over the shallow well region which is smaller than a distance required by a shallow well implantation design rule, and the emitter mask having a second opening located elsewhere which is larger than the shallow well implantation design rule;

selectively implanting ions of the second conductivity type into the shallow well region and into another region of the second conductivity type through the openings in the emitter mask, resulting in two distinct implanted regions, wherein a first region resides in the shallow well region and a second region resides elsewhere in the substrate;

thermally processing the substrate, wherein the implanted regions undergo diffusion to form an emitter region of the second conductivity type within the shallow well region of the first conductivity type and a shallow well region of the second conductivity type elsewhere, wherein a depth of the emitter region is

less than a depth of the shallow well regions of the first and second conductivity types, respectively.

21. The method of claim 20, further comprising selectively performing a source/drain implant of the second conductivity type into the emitter region, the source/drain implant forming an emitter contact region within the emitter region of the bipolar transistor.

22. The method of claim 21, further comprising selectively performing a source/drain implant of the first conductivity type into the shallow well region of the first conductivity type, thereby forming a base contact region within the base region of the bipolar transistor.

23. The method of claim 20, wherein the first conductivity type comprises p-type and the second conductivity type comprises n-type, wherein the transistor comprises an NPN bipolar transistor having an emitter region formed by a shallow N-well implant within a shallow P-well base region, and wherein a depth of the emitter region is less than a depth of the base region, and wherein a difference in the depths influences a gain of the bipolar transistor.